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PULSE INSTRUMENTS COMPANY

USER'S REFERENCE MANUAL

MODEL PI-451A

PULSE DRIVER

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## I. GENERAL DESCRIPTION

The PI-451A Programmable Pulse Driver is a plug-in unit designed to operate in the Tektronix TM-500 series power modules. It is compatible with other Pulse Instruments and Tektronix TM-500 series plug-ins operating in standard (non-custom wired) power modules.*

The PI-451A is a programmable level shifter as well as a triggered Pulse Generator. It accepts a low level TTL input pulse, and produces a high level 50 ohm output pulse for driving capacitive or resistive loads. It is especially well suited for driving MOS/CCD type devices in automatic testing applications.

As a level shifter-pulse driver, the output pulse width and pattern are determined by the input signal. But as a triggered pulse generator, the PI-451A generates output pulses with pulse delay and width variable from 100ns to 100$\mu$s.

In either mode of operation, the output open circuit high and low levels are independently manual adjustable or voltage programmable over a $\pm$ 25V range, with maximum output swing limited to 30V $\pm$ 3V. Output transition times are manually variable from 2ns/V to over 2$\mu$s/V. Option 002 provides digitally programmable output high and low levels, an ORed rear input, and a rear output which can be switched in parallel with the front output.

The voltage programming feature provides over voltage protection capatibility in testing CMOS devices, where the Vcc supply can be used to limit and track the output high level or amplitude.

Because of its compactness and versatility, the PI-451A can be used in a variety of applications, ranging from device characterization in the research lab to automatic testing in production.

* Do not force plug-in unit into non-campatible custom wired power modules (identified by non-matching barriers on edge connector inside power modules).

CAUTION: Turn power module off before inserting or removing the plug-in unit; otherwise, damage may occur to the plug-in circuitry.

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## II. SPECIFICATIONS

**OUTPUT HIGH LEVEL** — +25V to -24V open circuit, +12.5V to -12V into 50 ohms, manual control or external programming selectable by front panel switch

- Manual — Continuously variable by front panel control
- Voltage Programming — +25V to -24V. Open circuit offset voltage ≤80mV for positive going transition times set to ≤X1 and may increase to 125mV maximum for transition times >X1

**OUTPUT LOW LEVEL** — -25V to +24V open circuit, -12.5 to +12V into 50 ohms, manual control or external programming selectable by front panel switch

- Manual — Continuously variable by front panel control
- Voltage Programming — -25V to +24V. Open circuit offset voltage ≤ 80mV for negative going transition times set to ≤X1 and may increase to 125mV maximum for transition times >X1

**OUTPUT AMPLITUDE** — 1V min. to 30V ±3V max. open circuit, 0.5V min. to 15V ±1.5V max. into 50 ohms.

**OUTPUT LEVEL MONITORS** — Two banana jacks are provided for monitoring output High and Low levels in the Manual or Digital Program mode and for setting the output levels in the Voltage Program mode. Offset voltages are identical in all cases

**OUTPUT TRAMSITION TIMES** — 2ns/V to 2us/V at 25V amplitude and $C_L$ = 100pf, continuously variable by 3 position range switch and independent leading and trailing edge controls. When driving a 50 ohm load, transition edges may exhibit exponential rather than linear characteristics

**MAX OUTPUT REPITITION RATES (3ft length 50 ohm cable from front panel output only)**

| Capacititive Load ($C_L$) | $f_{max}$ @ 20V Amplitude | $f_{max}$ @ 25V Amplitude |
|---|---|---|
| 20pf | 10 MHZ | 8.5 MHZ |
| 100pf | 8 MHZ | 7 MHZ |
| 300pf | 5 MHZ | 4 MHZ |

**OUTPUT SETTLING TIME** — Approximately 750us to o.1% of full scale for either analog or digital programming inputs when output transition times are set to minimum

**OUTPUT ABERRATIONS** — 5% + 200mV P-P for output amplitude greater than 3V while driving a 3ft length of 50 ohm cable terminated into 100pf // 1 Meg-ohm

**OUTPUT POLARITY** — Normal or inverted output selectable by front panel switch

**OUTPUT PULSE DELAY** — Output pulse delay is 15ns maximum with respect to trigger output or is adjustable from less than 100ns to greater than 100us in 3 decade steps plus a 10 to 1 continuously

| | |
|---|---|
| | variable control when DELAY/WIDTH switch is pulled. 2V, 20ns pulse width min. required to trigger DELAY circuit |
| OUTPUT PULSE WIDTH | Output pulse width controlled by input or adjustable from less than 100ns to greater 100us in 3 decade steps plus a 10 to 1 continuously variable control when DELAY/WIDTH switch is pulled. 2V, 20ns pulse width min. required to trigger WIDTH circuit |
| TRIGGER OUTPUT | TTL compatible. Propagation delay from input 100ns maximum. Trigger output pulse width controlled by input |
| TTL INPUT | Front panel BNC connector, 2 - 5V into 500 ohms. |

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## III. FRONT PANEL CONTROLS

1. POWER - indicates power is on
2. OUTPUT LOW LEVEL - controls output Low Level in MANUAL MODE. Output low level must be set more negative than output high level; otherwise, no output will appear
3. OUTPUT HIGH LEVEL - controls output high level in MANUAL MODE. Output high level must be set more positive than output low level; otherwise, no output will appear
4. OUTPUT - output BNC connector. Open circuit voltage $\pm$25V
5. GROUND - system GROUND
6. LOW LEVEL INPUT/MONITOR - Dual function banana jack. Output low level voltage can be monitored in MANUAL and DIGITAL PROGRAM MODES and can be programmed by external voltage in the $V_{PROGRAM}$ MODE
7. HIGH LEVEL INPUT/MONITOR - Dual function banana jack. Output high level voltage can be monitored in MANUAL and DIGITAL PROGRAM MODES and can be programmed by an external voltage in the $V_{PROGRAM}$ MODE
8. MODE - selects manual or remote programming of output High and Low levels. DIGITAL PROGRAM position provided for unit with option 002 only
9. INPUT - input BNC connector. Accepts TTL compatible input signals. Input impedance 500 ohms
10. DELAY control - provides greater than 10 to 1 delay variation in any given range setting. DELAY control active only when DELAY/WIDTH switch (11) is pulled
11. WIDTH control/PULL switch - provides greater than 10 to 1 width variation in any given range setting. WIDTH control active only when it is pulled; otherwise, output pulse width controlled by input
12. DELAY range selector switch - selects range of output delay, 100ns, 1us or 10us when DELAY/WIDTH switch is pulled
13. WIDTH range selector switch - selects range of output pulse width, 100ns, 1us or 10us when DELAY/WIDTH switch is pulled
14. ⌐ TRANSITION TIME - controls positive going output transition time and provides continuous 10 to 1 transition time variation for every range setting
15. ¬ TRANSITION TIME - controls negative going output transition time and provides continuous 10 to 1 transition time variation for every range setting
16. TRANSITION TIME (ns/V) - selects output transition time ranges, 2ns/V, 20ns/V or 200ns/V
17. TRIGGER OUTPUT - provides TTL compatible output for triggering oscilloscope or other pulse driver. Trigger output pulse width contolled by input

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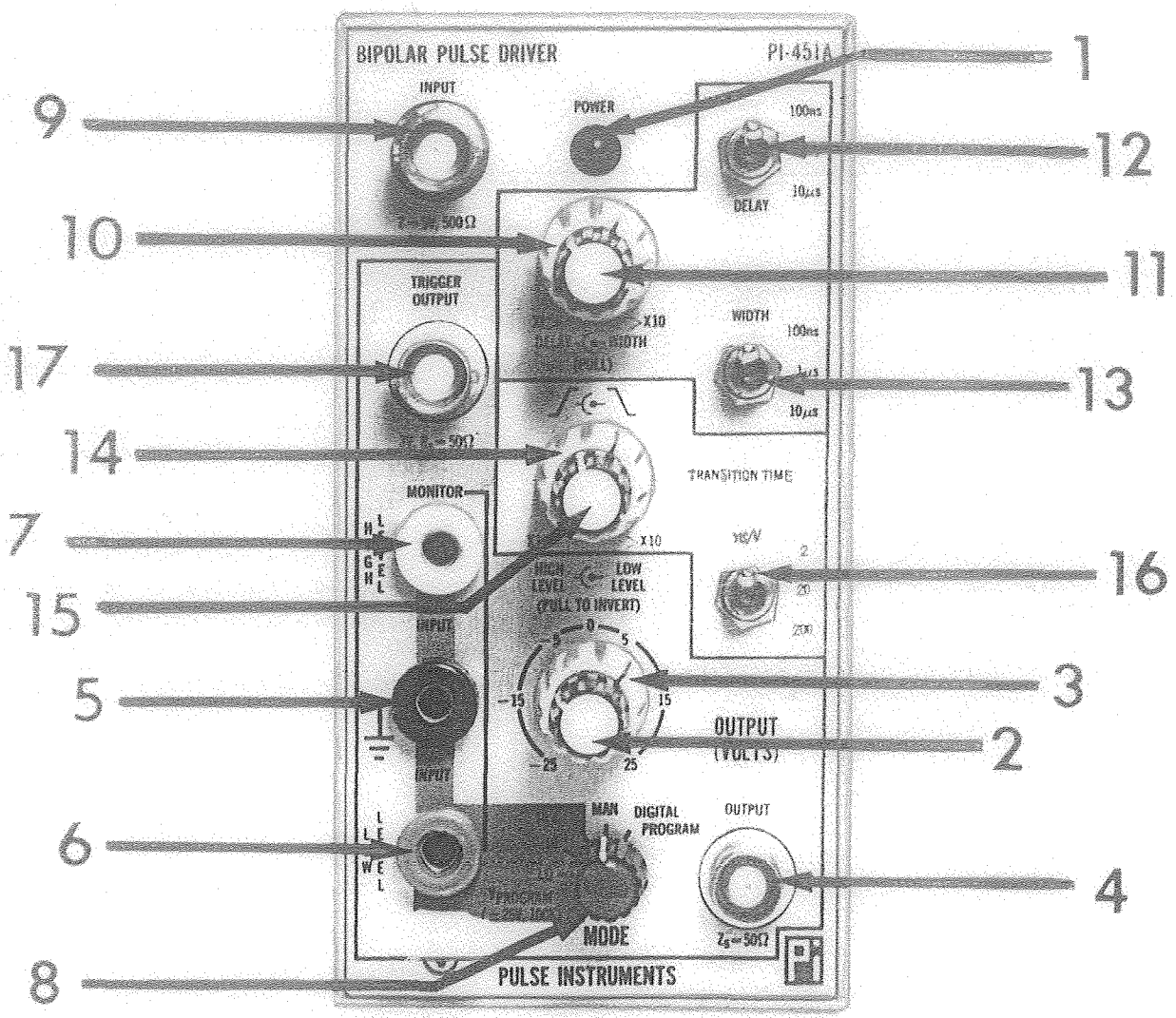


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## IV. PERFORMANCE CHECK/CALIBRATION PROCEDURE

### INTRODUCTION

The PI-451A, except for option 002, contains no internal adjustments. Power supply values are set using precision resistor dividers. Consequently, no calibration will be required. However, the following tests are recommended to ensure proper operation of the unit when it is received.

### TEST EQUIPMENT

The following equipment and accessories are required for checking the PI-451A. Special fixtures, when specified, are used mainly for simplifying the test setup and procedure. They are available from Pulse Instruments Co.

DC-50MHz Oscilloscope with 20pf input capacitance.
4½ digit DVM
Pulse Generator
0-25V Power Supply
50 ohm feed through termination
3ft. length RG-58CU (50 ohm) coaxial cable (3)
BNC Tee Connector
BNC to bannana jack adapter
82pf load

### WARM-UP

Allow the unit to operate in a TM-500 series mainframe for approximately 15 minutes before checking and calibrating it.

1. CHECK MAXIMUM OUTPUT HIGH LEVEL

1.1 Set Mode switch to MANUAL.

1.2 Set output to INVERT by pulling out the LOW LEVEL control knob.

1.3 Set transition time controls to FCCW positions.

1.4 Connect negative terminal of DVM to front panel bannana ground jack and positive terminal to output BNC connector using the BNC-bannana jack adapter.

1.5 Turn output HIGH LEVEL control to +25V (FCW) and output LOW LEVEL control to approximately +5V. (High level setting minus low level setting must be less than 27V.)

1.6 Check for +25V minimum output level open circuit and 12.5V min. into 50 ohms.

2. CHECK MINIMUM OUTPUT HIGH LEVEL

2.1 Turn both output HIGH and LOW LEVEL controls to -25V (FCCW).

2.2 Check for -24V maximum output high level open ckt and -12V min. into 50 ohms.

2.3 Set output high level to approximately -5V.

3. CHECK MINIMUM OUTPUT LOW LEVEL

3.1 Push in LOW LEVEL control knob (output not inverted).

3.2 Check for -25V maximum output low level open circuit and -12.5V min. into 50 ohms.

4. CHECK MAXIMUM OUTPUT LOW LEVEL

4.1 Turn both output HIGH and LOW LEVEL controls to +25V (FCW).

4.2 Check for +24V minimum output low level open circuit and +12V min into 50 ohms.

5. CHECK OUTPUT OFFSET AND VOLTAGE PROGRAMMING

5.1 Set Mode switch to the HI and LO position of the V program mode.

5.2 Apply a -25V DC voltage to the LOW LEVEL input jack.

5.3 Connect positive terminal of the DVM to the -25V source and negative terminal to the PI-451A output.

5.4 Set the negative going transition time control (smaller knob) to the FCCW position, and check for ±80mV maximum output low level offset.

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5.5 Slowly rotate the negative going transition time control to the FCW position, and check for +125mV maximum output low level offset.

5.6 Set the transition time control to obtain maximum output offset.

5.7 Slowly vary the input voltage from -25V to -1V, and check for ±125mV maximum output offset. Disconnect the negative input voltage.

5.8 Set output to INVERT by pulling out the LOW LEVEL control knob.

5.9 Apply a +25V DC voltage to the HIGH LEVEL INPUT jack.

5.10 Connect positive terminal of the DVM to the +25V source.

5.11 Set the positive going transition time control to the FCCW position, and check for ±80mV maximum level output offset.

5.12 Slowly rotate the positive going transition time control to the FCW position, and check for ±125mV maximum high level offset.

5.13 Set the transition time control to obtain maximum output offset.

5.14 Slowly vary the input voltage from +25V to +1V, and check for ±125mV maximum output offset.

## 6. CHECK OUTPUT TRANSITION TIMES

6.1 Set Mode switch to MANUAL.

6.2 Push in output LOW LEVEL control knob.

6.3 Set both transition time controls to the FCCW positions and range switch to 2ns/V.

6.4 Connect a positive going, 2V pulse to the input BNC connector using a 3ft. length 50 ohm coaxial cable.

6.5 Connect the PI-451A output to a 50 MHz oscilloscope using a 3 ft. length, 50 ohm coaxial cable, and terminate a 82pf, ±5%, capacitor at the input of the oscilloscope.

6.6 Adjust output high and low levels to ±12.5V, respectively, and obtain a scope display of exactly 5cm.

6.7 Check the 10%-90% positive and negative going transition times as shown in Table I.

## 7. CHECK MAXIMUM OUTPUT REPETITION RATE AND MINIMUM PULSE WIDTH

7.1 Set output High and Low Levels to ±10V, respectively, and obtain a scope display of exactly 4cm.

7.2 Set output transition times to minimum.

7.3 Set input signal repetition rate to approximately 1MHz.

7.4 Reduce input pulse width to obtain a minimum width, 20V, flat top output pulse.

7.5 Slowly increase input repetition rate and check for 8MHz minimum output repetition rate (It may be necessary to readjust input pulse width to obtain maximum output repetition rate).

7.6 Invert the output and check for 8MHz minimum output repetition rate.

7.7 Remove the 82pf load and reduce input repetition rate to approximately 100KHz.

7.8 Check for 50ns maximum pulse width at 50% points.

## 8. CHECK VARIABLE OUTPUT PULSE DELAY

8.1 Connect both trigger output and main output to the oscilloscope inputs using a pair of 3 ft. length, 50 ohm cables.

8.2 Set DELAY range to 100ns.

8.3 Pull DELAY/WIDTH control switch and set DELAY control to the FCCW position (X1).

8.4 Set input pulse amplitude to 2V and width to 20ns at the 1.5V level.

8.5 Check for 100ns maximum delay between the 1.5V point of the leading edge of the trigger output and the 50% point (0V) of the leading edge of the main output.

8.6 Turn DELAY control to the FCW position (X10).

8.7 Check for 1μs minimum output delay.

8.8 Repeat measurements for the 1μs and 10μs range positions.

## 9. CHECK VARIABLE OUTPUT PULSE WIDTH

9.1 Set WIDTH range to 100ns.

9.2 Set WIDTH control to the FCCW position (X1).

9.3 Check for 100ns maximum output pulse width at the 50% points (0V).

9.4 Turn WIDTH control to the FCW position (X10).

9.5 Check for 1μs minimum output pulse width.

9.6 Repeat measurements for the 1μs and 10μs range positions.

10. CHECK INSERTION OUTPUT PULSE DELAYS

10.1 Push in DELAY/WIDTH Switch.

10.2 Adjust input pulse width to 100ns.

10.3 Check for 15ns maximum delay from the leading and trading edges of the trigger output to those of the main output.

10.4 Disconnect the trigger output to the oscilloscope.

10.5 Using a BNC Tee connector and an additional 3 ft. length 50 ohm cable, connect the input signal from the PI-451A input BNC connector to the oscilloscope with a feed through 50 ohm termination.

10.6 Adjust input pulse amplitude to 2V.

10.7 Check for 110ns maximum delay from the leading and trailing edges of the input pulse to those of the main output.

11. CHECK OUTPUT ABERRATIONS

11.1 Set output High and Low levels to $\pm$1.5V, respectively.

11.2 Set output pulse width to 1$\mu$s.

11.3 Reconnect the 82pf load as in 6.5.

11.4 Check for maximum 0.35V P-P output aberrations.

12. CHECK MAXIMUM OUTPUT AMPLITUDE

12.1 Set output High and Low levels to approximately $\pm$15V, respectively.

12.2 Check for 27V minimum output amplitude open circuit and 13.5V minimum into 50 ohms.

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TABLE I. TRANSITION TIME CHECK

| Transition Time Setting | Approximate Pulse Width Required | Scope Time Base Setting | 10%-90% Output Transition Times |
|---|---|---|---|
| 2ns/V x 1 | 250ns | 0.05us | ≤ 40ns |
| 2ns/V x 10 | 2.5us | 0.5us | ≥ 400ns |
| 20ns/V x 1 | 2.5us | 0.5us | ≤ 400ns |
| 20ns/V x 10 | 25us | 5us | ≥ 4us |
| 200ns/V x 1 | 25us | 5us | ≤ 4us |
| 200ns/V x 10 | 250us | 50us | ≥ 40us |

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# DIGITAL PROGRAMMING OF OUTPUT LEVELS (DAC) - OPTION 002

## I. INTRODUCTION

This factory installed option adds digitally programmable output High and Low level controls to the standard PI-451A Pulse Driver. An additional TTL clock input and a High Level output are provided. These clock input and output together with the digital programming inputs are accessible only through the rear edge connector of the plug-in unit. Consequently, a Tektronix TM-506 power module with option 02 and with Pulse Instruments MOD-DP custom inter-compartmental wiring is required in order to obtain these added features. The PI-451A-002 digitally programmable Pulse Driver can also be used with any standard TM-500 series power module, but it will function only as a manually controlled unit.

The digitally programmable output level controls enable the PI-451A-002 to be interfaced with computer control systems for performing automatic testing.

## II. FRONT PANEL CONTROLS

The PI-451A-002 front panel controls are identical to those in the standard unit except that the MODE switch is provided with the additional DIGITAL PROGRAM position. In this position, the manual level controls are disconnected, and the digital inputs applied to the rear edge connector control the output levels. The front panel banana jacks remain in the monitor mode.

## III. DIGITAL PROGRAMMING INPUTS

Digital programming inputs to the PI-451A consist of 16 lines, and they are low power schottky TTL compatible:

$D_1$ - output level polarity ($\overline{\text{positive}}$/negative)
$D_2$ - $D_{12}$ - output level magnitude (see truth table for typical values)
$\overline{PS}$ - plug-in select
$\overline{MS}$ - mainframe select
LS - output level select (Hi level/$\overline{\text{Lo level}}$)
DS - data strobe

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P1-451-002 OUTPUT LEVEL TRUTH TABLE (Typical Values)

| $D_1$ ± | $D_2$ 12.5V | $D_3$ 6.25V | $D_4$ 3.125V | $D_5$ 1.563V | $D_6$ 781.3mV | $D_7$ 390.6mV | $D_8$ 195.3mV | $D_9$ 97.66mV | $D_{10}$ 48.8mV | $D_{11}$ 24.4mV | $D_{12}$ 12.2mV | OUTPUT LEVEL |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 24.9875V |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 24.9021V |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 23.9995V |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 23.9018V |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 12.50 V |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 10.0097V |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 6.25V |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1.563V |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1.001 V |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0.3906V |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.0122V |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.00 V |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -0.0122V |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | -0.3906V |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | -1.001V |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -1.563V |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -6.25V |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | -10.0097V |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -12.50 V |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | -23.9995 V |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -25.00V |

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1. Input Sequence

No special loading sequence is required; either the Hi level or Lo Level DAC may be loaded first. Output High Level must be more positive than Output Low Level; otherwise, no output will appear. Input data is loaded into the selected plug-in unit following the LOW to HIGH transition of the DATA STROBE (DS) input.

2. Input Code

Complementary offset Binary: This code is obtained by first complementing the straight binary code ( 000 --- 0 = zero, 111 --- 1 = FS) and then subtracting from it the mid scale value of the straight binary code ( 1000 --- 0). Typical values of a number of positive and negative output levels are given in the OUTPUT LEVEL TRUTH TABLE.

The binary word required for generating a positive output level $V_{0+}$ can be obtained by using the equation:

$$V_{0+} = \bar{a}_1 + \bar{a}_2 D_2 + \text{----} \bar{a}_{12} D_{12} = \bar{a}_1 + \sum_{i=2}^{12} a_i D_i ,$$

where $D_i$ represents the weight of a given bit as shown in the truth table, and $\bar{a}_i$ is the binary coefficient. $\bar{a}_1 = 0$ for positive or zero output levels, and $\bar{a}_i = 1$ for negative output levels.

For a given value of $V_{0+}$, say 10.0097V, the required terms in the equations are first identified ($D_3$, $D_4$, $D_7$, $D_8$, and $D_{10}$). The corresponding coefficients ($a_1$, $a_3$, $a_4$, $a_7$, $a_8$, and $a_{10}$) are then set equal to zero and the remaining ones to one. The resultant binary word is:

| | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_8$ | $D_9$ | $D_{10}$ | $D_{11}$ | $D_{12}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W= | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |

When this binary word is connected to the corresponding data bits of the PI-451-002 MOS/CCD driver, the selected output level (Hi or Lo) will be 10.0097V $\pm$ 100mV max. If a negative output level, say -10.0097V, is desired, the binary word required is obtained from $\bar{W} - 1$ or

$$\begin{array}{r} 1\ 0\ 1\ 1\ 0\ 0\ 1\ 1\ 0\ 1\ 0\ 0 \\ -)\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1 \\ \hline 1\ 0\ 1\ 1\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 1 \end{array}$$

In other words, to find the binary input for a negative output level, first determine the input for the corresponding positive output, complement it and then subtract 1. The result is the binary word required for generating the negative output level.

## IV. REAR TTL CLOCK INPUT

One additional TTL clock input is added to the rear connector. This rear input is ORed with, and is identical to, the plug-in front panel input.

## V. REAR PULSE DRIVER OUTPUT

One additional Pulse Driver output is added to the rear edge connector. An internal switch, mounted on the PC board, selects either front panel output only (F) or front and rear outputs connected in parallel (FR). Since the connection from the Pulse Driver output to the power module rear panel BNC connector is more than 3ft. long, it loads the front panel BNC connector when both outputs are connected in parallel. Therefore, when the switch is in the FR position, the front panel output should be used only as a monitor rather than a drive output. For minimum loading conditions, $C_L \leq 100pf$, transition time is 2.2ns/V min. vs 2ns/V min. for the front panel only output.

## VI. SPECIFICATIONS

Except for the parameters listed below, specifications for all other parameters are identical to the standard PI-451A.

| | |
|---|---|
| OUTPUT HIGH LEVEL | +25V to -24V, manual control, digital or voltage programming selectable by 5 position MODE switch. |
| DIGITAL PROGRAM | Resolution: 11 bits (12mV typical) plus sign bit. Accuracy: $\pm$100mV of programmed value for positive going transition time set to $\leq$ x 1 and may increase to 125mV maximum for transition times $>$ x 1. |

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| | |
|---|---|
| OUTPUT LOW LEVEL | -25V to +24V, manual control, digital or voltage programming selectable by 5 position MODE switch. |
| DIGITAL PROGRAM | Resolution: 11 bits (12mV typical) plus sign bit. Accuracy: ±100mV of programmed value for negative going transition time set to ≤ x 1 and may increase to 125mV maximum for transition times > x 1. |
| REAR OUTPUT TRANSITION TIMES | 2.2ns/V to 2.0us/V at 25V amplitude and $C_L$ = 100pf, continuously variable by 3 position range switch and independent leading and trailing edge controls. |
| REAR OUTPUT MAXIMUM REPETITION RATES | 10% or less lower than those specified for the front output. |

| SIZE | CODE IDENT NO. | DRAWING NO. |
|---|---|---|
| | | 91000121 |
| SCALE | | SHEET 5 |

## VII. PERFORMANCE CHECK/CALIBRATION PROCEDURE

### INTRODUCTION

The PI-451A Pulse Driver with Option 002 has been calibrated and checked prior to shipment. Consequently, no additional calibration will be required. If calibration is found to be necessary, the following procedure should be used. The only calibration required consists of setting correctly the full scale maximum and minimum values of the output High and Low levels. If performance check only is desired, the adjustment portion of the procedure should not be used.

### TEST EQUIPMENT

The following equipment and accessories are required for checking and calibrating the PI-451A-002. Special fixtures, when specified, are used mainly for simplifying the test set up and procedure. They are available from Pulse Instruments Co.

DC-50MHZ Oscilloscope
5½ digit DVM
Pulse Generator
0-25V Power Supply
3ft. length RG-58CU (50 ohm) coaxial cables (2)
BNC to banana jack adapter
PI-810 Manual Programming Box (99000160)*
TM-506 Power Module with Option 02 and with Pulse Instruments MOD-DP.

### WARM-UP

Allow the unit to operate in a modified TM-506 power module for at least 25 minutes before checking and calibrating it.

* Special fixture

## 7.1 SET UP AND PRELIMINARY CHECK

7.11 Units with Digital Programming Option (002) can be calibrated only in a specially wired TM-506 power module (Pulse Instruments MOD-DP*). In addition, a means of loading a 16 bit binary word (such as the Pulse Instruments Manual Programming Box, PI-810) into the rear panel 50 pin connector is required. In order to facilitate calibration, three plug-in units inserted in slots 1, 3, and 5 can be calibrated simutaneously.

7.12 Briefly verify that the Digital Program mode is functioning by loading in a set of convenient high and low levels (see Table). Be sure that no signal is connected to the TTL input.

7.13 Set transition time controls to minimum (FCCW).

## 7.2 OFF SET ADJUSTMENT ** ($R_{142}$/HLOS and $R_{145}$/LLOS)

7.21 Set output Low Level to -25.00V and output High Level to -23.9995V. (See Table for correct codes).

7.22 Adjust LOW Level off set $R_{145}$ until output low level is -25.00±2mV.

7.23 Set output to INVERT and adjust HIGH LEVEL OFF SET $R_{142}$ until ouput high level is -24.0V±2mV.

## 7.3 GAIN ADJUSTMENT ** ($R_{143}$/HL Gain and $R_{144}$/LL Gain)

7.31 Set High Level to +24.875V and Low Level to 23.995V (shown in Table).

7.32 Set output to INVERT and adjust High Level Gain $R_{143}$ until output High Level is 24.9875V±2mV.

7.33 Set output to Normal and adjust Low Level Gain $R_{144}$ until output Low Level is 23.995V±0.2mV.

7.34 Repeat steps 7.21 through 7.33 several times until the end points are calibrated.

* Other equivalent MOD's mode prior to 1982 consist of MOD451, 451A, 454 and 454A.

** A small flash light will help in locating in adjustment screws in the trim pots.

| SIZE | CODE IDENT NO. | DRAWING NO. 91000121 |
|---|---|---|
| SCALE | | SHEET 7 |

## 7.4 CHECK HIGH LEVEL MID SCALE

7.41 Set Low Level to -1.563V and High Level to 0.000V.

7.42 Set output to INVERT. If output is within ± 35mV, the high level circuit is calibrated. If not, go to 7.43.

7.43 If output is positive, adjust gain control $R_{114}$ to reduce ½ its value and adjust off set control $R_{113}$ to reduce the remaining half. If output is negative adjust $R_{113}$ first and then $R_{114}$. Zero level shall be set to within ± 35mV.

7.44 Check and record all positive values of High Level setting as shown in Table, and they shall be within ± 75mV. If not, the entire procedure involving High Level calibrations must be repeated.

7.45 Set Low Level to -25V. Check and record all negative values of High Level setting, except -25V, as shown in Table. They should be within ±75mV.

## 7.5 CHECK LOW LEVEL MID SCALE

7.51 Set High Level to +1.563V and Low Level to 0V.

7.52 Set output to Normal. If output is within ±35mV, the Low level circuit is calibrated. If not, go to 7.53.

7.53 If output is positive, adjust gain control $R_{112}$ to reduce ½ its value and adjust off set control $R_{111}$ to reduce the remaining half. If output is negative, adjust $R_{111}$ first and then $R_{112}$. Zero level shall be set to within ± 35mV.

7.54 Check and record all values of Low Level setting as shown in table, and they shall be within ± 75mV. If not, the entire procedure involving Low Level calibration must be repeated.

7.55 Set High Level to +24.9875V. Check and record all positive values of Low Level setting, except 24.9875V and 24.9021V, as shown in Table. They should be within ± 75mV.

## 7.6 CHECK REAR INPUT AND MINIMUM OUTPUT TRANSITION TIMES

7.61 Set internal "F-FR" slide switch to "FR".

7.62 Apply a 2V input to the rear input BNC connector, marked "TTL CLOCK INPUT".

7.63 Connect the rear output "A" BNC connector marked "CCD CLK AND POWER SUPPLY OUTPUT" to the oscilloscope and terminate it with an 82pf load at the scope input.

7.64 Adjust output HIGH and LOW levels to $\pm$12.5V, respectively, and obtain a display of exactly 5cm.

7.65 Set transition times to 2ns/V x1 (FCCW).

7.66 Check for maximum 44ns rise and fall times at the 10%-90% points.

7.67 Set "F-FR" slide switch to F, unless rear output is to be used.

| SIZE | CODE IDENT NO. | DRAWING NO. |
|---|---|---|
| | | 91000121 |
| SCALE | | SHEET 9 |