System 4700

Automated FPA System

The Pulse Instruments System 4700 Automated FPA Test System is the product of years of experience in the design of instrumentation and systems for the testing of CCDs, CMOS imagers, IR Detectors, and Focal Plane Arrays.

The system is flexible and expandable, with standard options and software that will allow your system to expand as your needs change.

The system can be enhanced with the addition of cards for different clock speeds, bias currents, four quadrant bias supplies (force voltage/limit current, force current/limit voltage function), and additional data acquisition channels to meet your specific requirements for low noise, speed and accuracy.

There are a variety of test heads available which are easily interchanged. The test configuration can be changed in minutes. The interface to the device under test (DUT) is a line of dewars and interface cards designed specifically for the Test System.

The purchase of a system includes training and installation by Pulse Instruments personnel to ensure you can start testing your parts within days of the arrival of the test system.

System 4700 Automated Test System

Design Concept

The System 4700 Automated FPA Test System is a low noise system that gains from Pulse Instruments' experience in the integration of test systems to meet the most stringent low noise test applications.

A host of programmable features make the system ideal for Research and Development, Characterization, and Production Testing.

All instruments in this system are controlled via IEEE-488 GPIB with the exception of the Data Acquisition System which is VME bus compatible for increased speed in data collection.

The Equipment Bays and Safety Features

Each equipment bay is stand alone with its own isolation transformer, power conditioning, emergency power interrupts, ground fault isolation, and circuit breakers.

The equipment, as presented in the standard configuration, will occupy part of the space in the three bays. Additional room is available for other test instruments that you may want to include, such as an oscilloscope.

A Computer desk with drawers provides additional rack space. For operator safety, each rack and the computer desk are equipped with emergency power off switches, which are large button switches that are easily accessible.

The system output interface is via a connector bulkhead panel located at a convenient location to interface to the device under test, dewar or test head.

Dewars manufactured by Pulse Instruments are preferred since the internal cards in the dewars have been designed to work with the system to provide the best possible drive waveforms and flexible low noise grounding schemes.

Analog Equipment Bay

The analog equipment bay houses the analog electrical stimulus consisting of the low noise DC bias supplies, the clock driver cards, Power Mainframe and Analog Power Mainframe (for the Acquisition Subsystem). This bay contains the low noise components of the system which connect directly to the device under test and is floating with respect to other equipment bays.

Digital Equipment Bay

The digital equipment bay houses the digital portion of the electronic stimulus module. It contains the control of the clock drivers and DC biases, the timing generator, a switching matrix, and additional equipment such as digital multimeters and oscilloscopes.

Access for monitoring all signal driver and DC bias lines are also located in this bay. This monitor panel can be automatically disabled when running a test or collecting data.

Timing Stimulus

Timing generation is provided by our new Data/Pattern Generator, the PI-2000. With up to 150 MHz operation, and a memory depth of 32K bits for each of 8 to 40 channels, the PI-2000 Data/Pattern Generator is a versatile digital signal source that can generate extremely long patterns. The instrument is also easy to program with our PI-PAT software.

Each channel has a memory depth of 32K bits with virtually unlimited levels of looping. As many as 2,730 repeatable subpatterns may be created and used within the program to produce extremely long data patterns.

DC Biases & Clock Drivers

The 4000 Series Low Noise DC Bias and Clock Driver System uses a mainframe approach that separates the digital electronics from the DC bias and clock driver cards, both optically and through the use of separate power sources.

The power required for the clock driver cards and DC bias cards, is supplied by dedicated DC power supplies that are located physically in the rack, but are not part of the Instrument Mainframes, which allows floating of the clock drivers and DC biases for noise reduction. Each clock driver and DC bias in the system is independently programmable.

Sequencing the application of the clock drivers and DC biases to the device under test, makes certain that voltages are applied or removed from the DUT pins in the safest order.

The clock drivers provide precise low noise performance with independently programmable high and low voltage levels; rise and fall times; optional Tri-Level outputs; and/or delay and width adjust, with speeds up to 65MHz.

A four Quadrant Bias Card provides two channels of Voltage/Current source per card. Each channel can be programmed independently as a fixed voltage or fixed current source.

Data Acquisition

Designed specifically for the acquisition of data from imaging devices like CCDs, IR Detectors and Focal Plane Arrays, the Data Acquisition System can acquire data at rates up to 40 MHz with 10 bit resolution or with up to 16 bit resolution at 2 MHz. The system is designed to have multiple acquisition cards in parallel collecting data at these rates. We have delivered systems with up to 16 channels in parallel.

Data Acquisition Cards

Each data acquisition card is complete with Global Offset Correction, Amplification, Filtering, Correlated Double Sampling, A/D Converter, and 16 Megabytes of RAM per channel.

All inputs to the data acquisition cards, and all outputs from the A/D converter are optically isolated to prevent outside sources of noise from entering the system.

Control of the data is through memory mapped access to the VME bus. The output of the A/D converter is stored as 16 words in a 32 bit structure for increased system speed.

An Area of Interest (AOI) feature is used for sub-image and multiframe acquisition. This feature will allow high speed processing and display of a window of the focal plane of any size up to 2048 X 2048 pixels.

Separate power supplies and ground systems are used for Analog and Digital circuitry on the data acquisition cards to further reduce noise.

Preamplifier

The PI-4007 is a four channel preamplifier packaged to set close to the device under test. The four channels can output data simultaneously, or be multiplexed into one channel to reduce the number of channels required.

Each channel has a single ended video input and a differential video output capable of driving 50 Ohm loads.

The input to the preamplifier will accept signals in the range of $\pm$ 15 V. This input is a programmable window that accepts a maximum signal level of $10V_{PP}$ while allowing at the same time, a correction of the DC offset of up to $\pm$ 10V to 16 bit accuracy.

The bandwidth of the preamplifier is $\geq$ 50 MHz, and the input referred noise is < 50nV/$\sqrt{}$Hz.